ABSTRACT

A method of evaluating a wafer structure formation process includes extracting the outline of an actual mask pattern, and simulating a lithographic process using the actual mask pattern to obtain a simulated wafer structure. The extracting the outline of the actual mask pattern may include, for example, imaging the actual mask using a scanning electron microscope (SEM). A second simulated wafer structure may also be obtained, by simulating the lithographic process using the ideal mask pattern design that was used in producing the actual mask pattern. Thus the relative contribution of mask pattern effects to overall wafer proximity effects may be evaluated by comparing the two simulated wafer structures, either with each other or against a benchmark such as a desired, ideal structure. This information may then be used to generate optical proximity correction (OPC) mask designs which compensate for mask patterning errors and give better wafer performance. The simulated wafer structures may be overlaid upon one another to allow for a direct comparison and full analysis of CD variations.